AC 2007-1053: A CAPSTONE ANALOG INTEGRATED CIRCUITS PROJECT FOR ELECTRONICS ENGINEERING TECHNOLOGY MAJORS

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A Capstone Analog Integrated Circuits Project for Electronics Engineering Technology Majors

Abstract

Oregon Institute of Technology offers a Bachelor of Science in Electronics Engineering Technology that includes a senior level capstone course in analog integrated circuit design. This course includes a two credit hour (six contact hours per week) laboratory in which students would normally perform six to eight individual “canned” experiments. Recently the author has re-structured the laboratory to become a term-long group project in the area of analog integrated circuits. This paper describes the results of one of these team projects.

Introduction

The objective of this capstone course is to expose senior EET majors to the design process for analog integrated circuits by working as a member of a design team. Upon completion of this course, a student will have been exposed to the processes of working in a team, picking an idea, researching the topic, formulating a design, dividing up the tasks, generating a schedule, writing periodic progress reports, doing hand calculations and computer simulations, breadboarding individual stages, integrating the entire system, and presenting their results in a formal oral presentation and a final written report; including a fully operational demonstration.

Requirements

The instructor stipulates that the design must be DC coupled (i.e. no coupling or bypass capacitors), that the breadboard must use matched transistor ICs such as the CA3046 and CA3096, and that the circuit should use current-mirror biasing, active loads, a differential input stage, a gain stage, a level shifter, and an output stage, if applicable. The major building blocks are npn and pnp bipolar junction transistors, but MOSFETs are also allowed.

Summary

To date, student teams have successfully demonstrated fully operational designs in breadboard for such analog circuits as operational amplifiers, instrumentation amplifiers, voltage comparators, digital-to-analog converters, analog-to-digital converters, sample-and-hold amplifiers, voltage controlled oscillators, phase-locked loops, a frequency synthesizer, and Costas loops. This paper summarizes the results of a team that developed a phase-locked-loop from the transistor level. The students worked harder and learned more compared to the canned lab approach, while the instructor worked less and felt very proud of his students.
Purpose and Objectives

The concept of a phase-locked loop was first developed in the 1930s. It has since been used in communications systems of many types. A phase-locked loop is a closed-loop feedback control system, and its main purpose is to maintain a generated signal in a fixed phase relationship to a reference signal. Until recently, however, phase-locked loop systems have been too costly and complex for most consumer and industrial markets where other approaches were more economical. However, the PLL is particularly useful to monolithic construction, and integrated-circuit phase-locked loops can now be fabricated at very low cost. Their use has become attractive for many applications including FM demodulators, stereo demodulators, tone detectors, frequency synthesizers, and the like.

The objective of this lab is to design and construct a phase-locked loop using only discrete components. The circuit must perform up to specific design requirements which are reasonable for PLL systems. The timeline for this project is less than 10 weeks.

Materials & Equipment

- CA3046 NPN Transistor array packages
- 6.2V Zenor Diodes
- Various Resistors
- Protoboard
- Agilent 33220A Function Generator
- Hewlett Packard 54600B Oscilloscope

Theory of Operation

A block diagram of a phase-locked loop system is shown below.

The basic elements of the PLL system are a phase detector, a loop filter, an amplifier, and a voltage-controlled oscillator (VCO). The VCO is simply an oscillator whose frequency is proportional to an externally applied voltage. When the loop is locked on an input signal, the VCO frequency is exactly equal to the input signal’s frequency. The output of the VCO is a
square wave regardless of what type of wave the input is. The phase detector basically works like a mixer which produces the sum and the difference frequencies between the input signal and the VCO signal. These signals are passed through a low pass filter which generates a dc or low-frequency signal proportional to the difference in phase between the two input signals. This is lastly fed into the VCO input which produces a correction frequency in order to maintain lock with the input frequency.

**Procedures**

The students constructed each of the following functional sections in the order listed. Each section was tested and proper operation was confirmed before proceeding to the following section.

Students were reminded that it is important when constructing these circuits on a breadboard to keep in mind certain layout considerations. Try to keep components as close as possible to minimize the length of connecting wires. This will improve the overall frequency response of the circuit. Keep wires neat and low to the board as well. This will keep the design cleaner and easier to troubleshoot when necessary. Use bypass capacitors across the supply voltages. For high frequency or capacitance sensitive oscilloscope measurements, use the x10 setting on the probe. Also, each CA3046 transistor array package has a substrate pin on the emitter of Q5 which must be tied to the lowest voltage seen by the package.

**Bias Circuitry Design**

The bias circuitry essentially creates the controlled voltage and current sources which provide bias and power to each of the functional components. This was constructed and verified first because its operation can easily be tested and is not dependent on any other functional section. Also, to test each of the other sections, various sources of bias current and voltage were needed from this circuitry.

Students designed and constructed the circuit as shown in the following Figure 2. They used +20V for the VCC supply.

When testing the above circuit alone, 10k ohm resistors were used as passive loads for the current sources. Each bias voltage and current were measured and came within +/- 10% of the following values:

\[
\begin{align*}
VCO_{Pwr} &= 7.0 \text{ V} \\
PD_{Pwr} &= 13.0 \text{ V} \\
PD_{VBias} &= 4.0 \text{ V} \\
PD_{IBias} &= 600 \mu\text{A} \\
CS_{IRef} &= 500 \mu\text{A} \\
VCO_{IRef1} &= 400 \mu\text{A} \\
VCO_{IRef2} &= 400 \mu\text{A} \\
VCO_{IRef3} &= 400 \mu\text{A} \\
VCO_{IRef4} &= 400 \mu\text{A}
\end{align*}
\]
Figure 2: Bias circuitry schematic for various bias currents and voltages.
Voltage Controlled Oscillator

The voltage controlled oscillator that the students built is shown in Figure 3. The (VCO) frequency is set by the value of the capacitor C1 and the sum of the currents that charge/discharge the cap. VCO_IRef1 and VCO_IRef4 are fixed at 400µA while the variable current sources VCO1 and VCO2 contribute up to 250 µA on each side. This creates an effective current range of 400 µA to 650 µA to charge or discharge the capacitor. Obviously, larger currents charge and discharge the capacitor faster and result in a higher output frequency.

The mechanism which controls the switching point of this circuit is R1 and Q1. The opposite side with R2 and Q4 is symmetric and operates identically except during the opposite half of each cycle. When enough current is drawn through the resistor, a sufficient voltage is created to turn on Q1. With Q1 on, enough current can flow to turn on Q5 and Q8. With Q8 on, the capacitor begins to charge at the rate of current from VCO_IRef1+VCO1. Eventually the voltage at the emitter of Q8 becomes higher than three V_{BE} drops from the VCO_Pwr voltage and the transistor turns off. At the same time the voltage on the other side of the capacitor has dropped below three V_{BE} drops and that side turns on which begins charging the capacitor in the opposite direction. The currents drawn from VCO1 and VCO 2 are controlled by a voltage, which is what makes this a voltage controlled oscillator.

The circuit as shown in Figure 3 was constructed. Necessary connections to the previously created current and voltage bias circuitry were made. The output at VCO3 or VCO4 was a 50% duty cycle square wave at around 100 kHz if VCO1 and VCO2 were not connected. The free-running frequency was higher due to the addition of these variable current sources.

The equation for finding the VCO operating frequency is,

\[
f = \frac{I_C}{4*C_1 * V_{BE(on)}}
\]

where \(I_C\) is the sum of the currents which charge or discharge one side of the capacitor, \(C_1\) is the value of the capacitor, and \(V_{BE(on)}\) is about 0.65V.

This equation is also used to calculate the VCO free-running frequency where \(I_C\) is specifically 400 µA + \(\frac{1}{2} (VCO1_{max})\), and \(VCO1_{max} = VCO2_{max} = \frac{1}{2} (CS_IRef)\) from Figure 2.
Phase Comparator

The phase comparator, shown in Figure 4, can be thought of as a high-gain mixer. Essentially, the input signal is exclusive OR’d (XOR) with the VCO signal so that the result is a square wave with a duty cycle proportional to the phase difference between the two signals. This is a high-gain circuit because the students wanted it’s output to be a square wave swinging rail-to-rail so that it’s specific DC average value is only dependent on it’s duty cycle. They did not want the amplitudes of either input waveform to affect the amplitude of the output. What this implies is that the amplitude of the input signal is not important, only it’s frequency and relative phase to the VCO input signal. It was observed that this circuit has the same output whether the input is 5 Vpk or 20 mVpk.

It was quite difficult for the students to verify proper operation of this circuit since the rest of the feedback circuitry had not been built yet. The only way to measure a constant frequency and duty cycle waveform on the output is to apply two phase shifted signals of identical frequency to the inputs. These are difficult waveforms to create using only the function generators. Instead, they used the VCO as one of the inputs and tried to closely match its frequency using a function generator. The results weren’t perfect but using the “Stop” function on the oscilloscope allowed them to freeze the screen to verify the correct output waveform.
**Filter & Level Shifter**

The output from the previous stage is a square wave with a duty cycle proportional to the phase difference between the two input waves. What is really wanted from this output signal is the DC average value of the wave. This is fed back into the VCO to generate the correction frequency. A nearly DC voltage can be recovered by passing the signal through a low-pass filter which allows only the relatively low frequency average on the output. A low-pass filter using a capacitor and the Thevenin equivalent resistance seen by the capacitor was built. The break frequency of the filter is given by,

$$ f_b = \frac{1}{2\pi R_{Th} C} $$

where $R_{Th}$ is the Thevenin equivalent resistance seen by the capacitor, and $C$ is the value of the filter capacitor.

Thevenin’s equivalent resistance seen by the capacitor can be approximated as $R_3 + R_4$ (see Figure 4), because the parallel path looking into the base of Q15 or Q16 (see Figure 5) is $r_e + (\beta+1)r_{(seen by emitter)}$ and can be considered negligibly large.

$$ R_{Th} @ R3+R4 = 15k\Omega $$
The break frequency should be low compared to the VCO free-running frequency, but not too low as to block the intended modulating frequency. For instance, if the goal is trying to recover modulated audio frequencies from a high-frequency FM signal, the filter break frequency should not be below several kHz, because then it would start filtering out the audio signal. Also, the PLL may have trouble tracking the input frequency if it is being modulated at a much higher frequency than the filter will pass. For simple testing purposes, the break frequency was set at approximately 1 kHz.

The level shifter, because of its emitter follower configuration, simply shifts the signal down by about 7V DC. This makes it the proper level to operate the voltage-controlled current sources shown in the next section.

![Figure 5: Schematic of Filter & Level Shifter. Filter capacitor is shown as C3.](image)

**Output & Voltage-Controlled Current Sources**

The voltage-controlled current sources are created as differential-input double paired transistor current sources. See Figure 6 for schematic. With no differential input, the current from the 500 µA constant source (CS_IRef) is split equally through R11 and R12. The current through R12 is then split equally between VCO1 and VCO2 which then feeds back to opposite sides of the capacitor in the VCO. As a differential voltage is applied to the bases of each transistor pair, the current from CS_IRef is steered to one side or the other. This increases or decreases the currents VCO1 and VCO2 which directly affect the frequency of the VCO.

Transistors Q2 and Q3 together act as a common emitter amplifier with the output voltage taken at their collectors. The gain of the amplifier is essentially:
\[ A_v = \frac{R_C}{r_e + R_E} = \frac{R_{13}}{r_e + R_{11}} \]

and \( r_e \) is found with zero input (\( I_E = 250 \mu A \)) as \( V_T/I_E \).

The resulting voltage gain is about 14. The output is then buffered by an emitter follower stage.

**Figure 6:** Schematic of output amplifier and voltage-controlled current sources. Note: R14 is shown to simulate the input impedance of another device connected to the output of the PLL.

**Summary of Results**

After complete construction, integration and testing, the phase locked loop **WORKED!!** The students had to make sure that their PLL held up to the initial specs which they initially predicted and attempted to achieve. It was also important that certain performance specs be tested and tabulated so that calculations could be made for the device to be used in other configurations or with other component values. Also, these values help to compare the student's discrete PLL with other known products.

Table 1 shows a comparison view of each calculated and measured specification. Another point of interest is to observe the capture and lock ranges for a specific point of operation. The “capture range” is the range of input frequencies to which the PLL can grab and lock on from a
free-running state. The “lock range” is the range of frequencies to which, once locked, the PLL can hold on. A graphical description is shown in Figure 7.

Note: All parameters were calculated or measured using the following values unless otherwise specified:

Supply Voltage: \( V_{CC} = 20\text{VDC} \)
VCO Capacitor: \( C_{VCO} = 1.52\text{nF} \)
Filter Capacitor: \( C_{filter} = 10\text{nF} \)
VCO \( V_{BE(on)} \): \( V_{BE(on)} = 0.6\text{V} \)

Table 1: Relevant calculated and measured device specifications.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Calculated</th>
<th>Measured</th>
<th>Units</th>
<th>Tolerance</th>
<th>Percent Difference</th>
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<tbody>
<tr>
<td>Dynamic Input Impedance</td>
<td>4.20</td>
<td>4.06</td>
<td>k( \Omega )</td>
<td>+/- 10%</td>
<td>3.33%</td>
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<tr>
<td>VCO Max Frequency (( C_{VCO}=1.52\text{nF} ))</td>
<td>180.6</td>
<td>187</td>
<td>kHz</td>
<td>+/- 10%</td>
<td>-3.54%</td>
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<td>VCO Free Running Frequency (( C_{VCO}=1.52\text{nF} ))</td>
<td>145.8</td>
<td>150.2</td>
<td>kHz</td>
<td>+/- 10%</td>
<td>-3.02%</td>
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<tr>
<td>AC Maximum Demodulated Output Voltage (( V_{p-p} )) **</td>
<td>3.80</td>
<td>4.00</td>
<td>V\text{p-p}</td>
<td>+/- 10%</td>
<td>-3.95%</td>
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<td>DC Demodulated Output Voltage (( V_{DC(ave)} )) **</td>
<td>17.35</td>
<td>17.15</td>
<td>V</td>
<td>+/- 10%</td>
<td>0.98%</td>
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<tr>
<td>Thevenin Filter Resistance - seen by filter capacitor (( R_{Th(filter)} ))</td>
<td>12.6</td>
<td></td>
<td>k( \Omega )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCO Sensitivity (( K_o ))</td>
<td>148</td>
<td>113.8</td>
<td>kHz/V</td>
<td></td>
<td>23.11%</td>
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<tr>
<td>Phase Detector Sensitivity (( K_D ))</td>
<td>2.68</td>
<td>2.50</td>
<td>V/Radian</td>
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<td>6.72%</td>
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<td>VCO Rise Time (10%-90%) **</td>
<td></td>
<td>230.5</td>
<td>ns</td>
<td></td>
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<tr>
<td>VCO Fall Time (90%-10%) **</td>
<td></td>
<td>110</td>
<td>ns</td>
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</table>
Conclusions

The students felt like this lab project was a great learning experience and an excellent opportunity to explore the inner workings of integrated circuits and especially phase locked loops. They gained in-depth knowledge of how phase locked loops work, and learned why certain parts of integrated circuits are made the way they are. For instance, why it’s important to use matched transistors on the same substrate when creating a current mirror.

The team members were fairly surprised how well each section of their circuit worked after being built. Very little needed to be changed from their original design. Also, the time spent troubleshooting each section was low in comparison to circuits built in other lab classes. The majority of the total troubleshooting time was spent solving trivial (but often frustrating) errors. These include the absence of a passive load when testing current sources, confusing measurements due to the oscilloscope probe being on the x10 setting, and accidentally not grounding the substrate pin on the transistor array packages. Beside these human mistakes, not much else was wrong with the actual circuit.

The circuit as a whole also had surprisingly great functionality as well. They closely met each of their predicted specs. Also, when actually set up to perform in real conditions – demodulating audio from an FM signal – the circuit operated as expected, and actually output a clear audio signal. This was quite gratifying for the students to see so much effort go into something that actually works like it was supposed to.

The measured specs for their device are on or around par with other phase locked loop systems which they researched. The maximum operating frequency of the entire circuit was naturally
lower than circuits built into a single monolithic chip simply because of longer connecting wires contributing to parasitic capacitance and noise.

According to the students, the phase-locked-loop project was a success as was shown in the FM audio demodulation demonstration, as well as in the measured specs. The students learned about phase-locked-loops, integrated circuits, and working as a member of a design team. A photograph of the actual completed breadboard is shown on the following page.

**Bibliography**

