

## **AC 2007-1073: A JITTER EDUCATION: AN ASSESSMENT OF THE FRESHMAN JITTER INTRO**

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## **A Jitter Education: An Assessment of the Freshman Jitter Intro**

### Abstract

This is the third in a series of papers addressing jitter analysis education in the Electrical Engineering Technology (EET) curriculum. The first paper, “A Jitter Education: Finding a Place for Jitter Analysis in the EET Curriculum,” described the basic types of jitter, their underlying causes, jitter measurements and displays (two related but distinctly different topics), and proposed a spiral approach to incorporate jitter analysis into a four-year EET curriculum.<sup>1</sup> The second paper, “A Jitter Education: An Introduction to Timing Jitter for the Freshman,” explained how to introduce the subject of timing jitter to a first-year EET student, as well as how Purdue University’s freshman curriculum lays a good foundation for understanding some jitter basics.<sup>2</sup> The focus of this installment is an assessment of the performance turned in by a “test class” of freshmen after an introduction to timing jitter in their second-semester digital electronics course.

### Introduction

The following excerpt, taken from the second paper in this series, applies equally well here.

“For the purpose of this paper, timing jitter is defined as ‘the phenomenon seen when a digital waveform’s transition appears before or after the expected time.’<sup>1</sup> When jitter displaces the signal’s transition so much that it happens in an adjacent clock cycle, the result is a data error on the bus. Because of the high speeds...of today’s systems, jitter that used to be negligible is now very significant, and can prevent a system from working correctly.<sup>1</sup> Today’s designers need the ability to analyze jitter, trace its root cause(s), and mitigate or eliminate the cause(s).

In order to effectively analyze jitter, one must understand its nature, the various measurements, how those measurements can be displayed, and the tools used to do the measurement and display. The first section provides a brief review of these jitter topics. For a more detailed discussion, see the first paper in this series and its source references.<sup>1</sup>

The premise of this series of papers is that it is preferable to teach jitter analysis a little at a time, in several courses, as students progress through their undergraduate curriculum. Given that approach, several topics are appropriate to work into one or more first-year courses, in order to lay a foundation for a more in-depth treatment in later years. The basis for this discussion will be the Electrical and Computer Engineering Technology (ECET) curriculum at Purdue’s College of Technology. Jitter analysis fits within Purdue’s ECET program objective outcome 3.1: Analyze, design, and implement electronic systems using control, communication, computer, or power systems.”<sup>2</sup>

Section two is a brief review of the subset of jitter topics that were taught. For more information concerning how Purdue's first year digital sequence prepares students to learn these jitter topics, please see the second paper in the series.<sup>2</sup> The third section describes how the assessment was done and the results. The final section draws conclusions from the results and suggests possible improvements

## Jitter Basics

Again, for the benefit of those who did not read the second paper in the series, the Jitter Basics section is repeated, below.

“There are two broad categories of jitter: random and deterministic. Random jitter (RJ) has a gaussian distribution with respect to time and is, therefore, unbounded. Some level of random jitter will always be present in a real system. Deterministic jitter (DJ), which has a bounded probability distribution, has several subcategories, and is generally caused by events over which the designer has at least some control. Examples of DJ include duty cycle distortion, periodic jitter, and intersymbol interference, each with its own root cause(s). The key to controlling these causal events is to first isolate the different types of jitter and trace each back to its source.

There are three primary jitter measurements.<sup>3</sup> Period jitter measures the time of each cycle in a waveform (not the same as periodic jitter, which is a type of jitter, not a measurement). Cycle-cycle jitter is the period difference between two adjacent clock cycles. Finally, time interval error (TIE) is the difference between the ideal and actual transitions of a signal.

Jitter can be displayed in several different ways. The histogram is a familiar technique for those wishing to view it as a probability distribution function. The trend waveform is a plot of jitter magnitude versus time. When displayed on the same plot with waveforms of interest, it can be used to correlate waveform events with jitter characteristics occurring at the same points in time. A third technique for viewing jitter measurements is the spectral display, which plots jitter magnitude on the vertical axis vs. frequency on the horizontal axis (i.e., a Fourier transform). It can be very useful for identifying sources of interference at known frequencies, such as a clock or high speed bus. A fourth method is the eye diagram, which is a great pictorial to show the size of a bus's data valid window, in both voltage and time. Finally, the bathtub curve, produced by a bit error ratio tester (BERT), is an indirect way of characterizing jitter.

Tools that can be used to measure timing jitter include the real time oscilloscope, sampling oscilloscope, logic analyzer, time interval analyzer, phase noise analyzer, and bit error ratio tester. The real time oscilloscope is by far the most ubiquitous of these, in both industry and academia, because of its general purpose utility and relatively low cost. Moreover, its frequent use by (Purdue) freshmen and sophomore

ECET students makes it the perfect basis for introducing early concepts of jitter analysis.”<sup>2</sup>

## Course Topics

The subject of timing jitter is covered in 30-45 minutes as part of one lecture during the second-semester digital electronics course. (The PowerPoint slides used for this portion of the lecture are shown in the Appendix.) First, timing jitter is defined, drawing a distinction between jitter and wander. This is followed by an explanation of the difference between random and deterministic jitter, with some graphical aids (created using MATLAB) to illustrate duty cycle distortion and intersymbol interference. Periodic jitter is explained without a graphical aid.

Next, the basic jitter measurements are described: period jitter, cycle-cycle and n-cycle jitter, and time interval error. Graphical aids generated with MATLAB are again used to illustrate these measurements, including the unit interval that must be derived to measure time interval error.

Finally, a couple of minutes is dedicated to explaining why a digital storage oscilloscope (DSO) is important to making the measurements (vs. an analog oscilloscope).

## Assessment Methodology and Results

The class consisted of only nine students and the course is only taught once per year, so it should be noted up front that there was no way to gather statistically significant results. Nevertheless, the learning objectives, exam questions, and exam results are worth reviewing.

The primary objectives for student retention were to:

- understand what timing jitter is;
- know that the two broadest categories of jitter are random and deterministic;
- comprehend the difference between random and deterministic jitter; and
- understand why a DSO is an important tool for measuring jitter.

The course had a total of four exams: three mid-semester exams and a comprehensive final. Exam 2 and the Final Exam both had questions covering jitter. Exam 2 had three multiple choice questions and one fill-in-the-blank, as shown in Figure 1 (answers c, d, d, and cycle-cycle, respectively).

Somewhat surprisingly, all nine students got questions 11-13 correct, and only one missed question 17, making the overall percentage for each question 100%, 100%, 100%, and 94.4%, respectively. This could indicate a good understanding of the material, or possibly that the questions are a bit too easy. Either way, it was encouraging to see such a strong showing.

11. The two most basic categories of timing jitter are
  - a. duty cycle distortion and time interval error.
  - b. unit intervals and intersymbol interference.
  - c. random and deterministic.
  - d. cycle-cycle and n-cycle.
12. In order to measure time interval error, the “ideal” clock must be reconstructed. The period of this “ideal” clock is called the
  - a. duty cycle.
  - b. pulse width.
  - c. step size.
  - d. unit interval.
13. An advantage of digital storage oscilloscopes (DSOs) over analog oscilloscopes is
  - a. the ability to store waveforms indefinitely.
  - b. the capability to store and display waveform points before the trigger.
  - c. the possibility of doing statistical analysis on accumulated data.
  - d. all of the above are advantages of DSOs.
17. The difference in period between two adjacent clock cycles of a waveform is called \_\_\_\_\_ jitter.

**Figure 1: Exam 2 Jitter Questions**

The Final Exam contained three multiple-choice questions, as shown in Figure 2 (answers c, d, and d, respectively). This time around, the questions were repeated exactly from Exam 2, and the results were the same: 100% for all three questions.

29. The two most basic categories of timing jitter are
  - a. duty cycle distortion and time interval error.
  - b. unit intervals and intersymbol interference.
  - c. random and deterministic.
  - d. cycle-cycle and n-cycle.
30. In order to measure time interval error, the “ideal” clock must be reconstructed. The period of this “ideal” clock is called the
  - a. duty cycle.
  - b. pulse width.
  - c. step size.
  - d. unit interval.
31. An advantage of digital storage oscilloscopes (DSOs) over analog oscilloscopes is
  - a. the ability to store waveforms indefinitely.
  - b. the capability to store and display waveform points before the trigger.
  - c. the possibility of doing statistical analysis on accumulated data.
  - d. all of the above are advantages of DSOs.

**Figure 2: Final Exam Jitter Questions**

## Conclusion

The results are encouraging, but with the benefit of 20/20 hindsight and more time for reflection, the data seem to suggest several adjustments to the exams are in order. First, although the students most likely understood it, their understanding of the *definition* of timing jitter was never explicitly tested. This could be remedied with a question asking them to define it, or to name it when given the definition. Alternatively, either the term or definition could be selected from a list (multiple choice).

Second, there was no question explicitly requiring the students to distinguish between random and deterministic jitter. A question could be added that lists several characteristics of either RJ or DJ, then requires the student to name it (fill in the blank), or select it from a list (multiple choice). Conversely, RJ or DJ could be given, and the student required to name its characteristics (short answer) or select them from a list (multiple choice).

Third, since three of the seven questions were repeated on the Final Exam, there were actually only four questions asked. Two of these “repeats” could be replaced with the questions described in the previous two paragraphs, without increasing the length of either exam. This would be a good idea, anyway. Given that the Final Exam questions were *identical* to three of the four Exam 2 questions, it is not surprising that the Final Exam questions were all answered correctly.

Fourth, it would be nice to add a lab experiment to reinforce one or more of the jitter concepts. One possibility might be to have the students design and construct a frequency divider circuit in the form of a counter that is clocked near its frequency limit. The output would first be measured directly, then measured after being passed through a simple “transmission line” circuit where it would be subjected to electromagnetic interference. The before and after frequencies would be compared, differences noted, and possibly, a bit error ratio calculated.

Fifth, the unusually high test results indicate that the questions might be too easy. Possible remedies include: changing the incorrect multiple-choice responses to words more similar to the correct answer; using fill-in-the-blank format instead of multiple choice; or giving the term and requiring the student to define it. Alternatively, at least to some degree, the results may reflect the author’s enthusiasm for the subject.

Finally, although there is room for improvement in the assessment methodology, the results are nevertheless encouraging. The basics of timing jitter appear to be well within the grasp of a second semester student, given the preparation provided in Purdue’s ECET curriculum.<sup>2</sup>

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<sup>1</sup> Harding, G. L. (2005). A Jitter Education: Finding a Place for Jitter Analysis in the EET Curriculum [CD-ROM]. *2005 Annual Conference Proceedings, American Society for Engineering Education.*

<sup>2</sup> Harding, G. L. (2006). A Jitter Education: An Introduction to Timing Jitter for the Freshman [CD-ROM]. *2006 Annual Conference Proceedings, American Society for Engineering Education.*

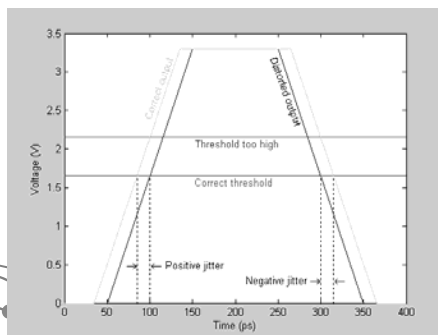
<sup>3</sup> Tektronix, Inc. (2003, October) *Understanding and Characterizing Timing Jitter* (Primer #55W-16146-1).

# Timing Jitter

- Transition appears early or late
- Wander: very slow jitter, formally 10 Hz or less
- Two fundamental types:
  - Random
  - Deterministic
- Measurements
  - Period jitter
  - Cycle-cycle and n-cycle jitter
  - Time interval error (TIE)

1

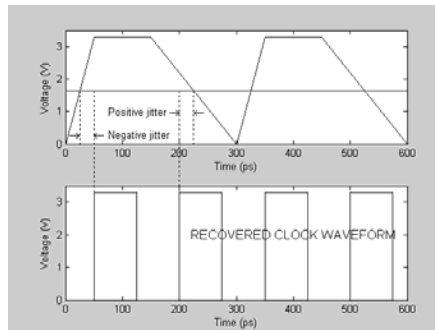
## Deterministic Jitter: Duty Cycle Distortion Causes



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Incorrect threshold voltage

### Asymmetric edge rates

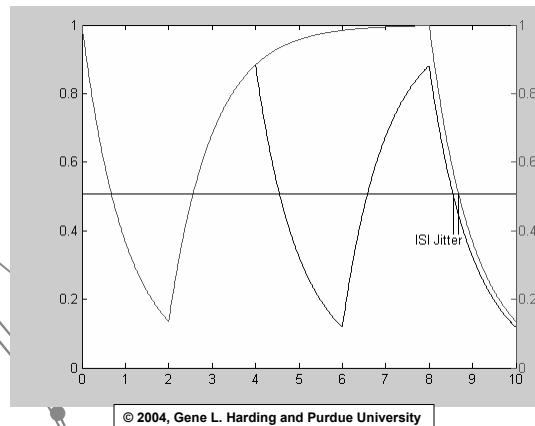


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## Appendix: Lecture Slides

### Deterministic Jitter: Intersymbol Interference Cause

Data path bandwidth too low



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### Deterministic Jitter: Periodic Jitter Cause

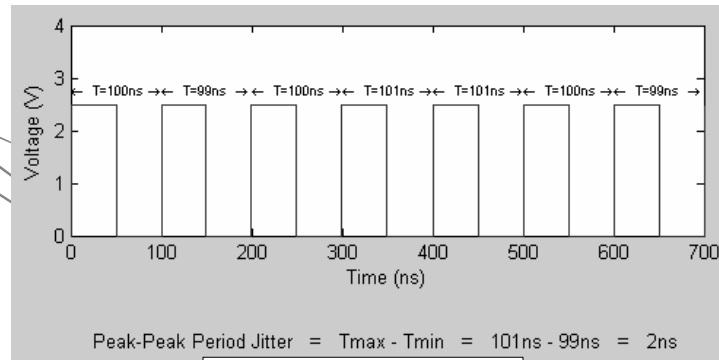
- Electromagnetic interference (EMI)
  - Correlated: from signal based on same clock
  - Uncorrelated: from signal based on a different clock

4

## Appendix: Lecture Slides

### Jitter Measurements: Period Jitter

- Measure each clock cycle in waveform
- Difference between max and min periods

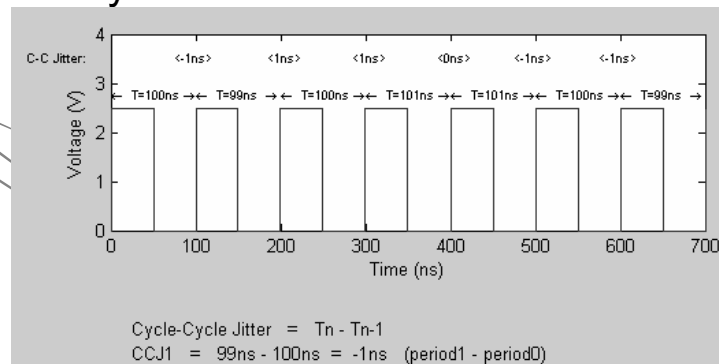


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### Jitter Measurements: Cycle-Cycle Jitter

- Derived from period jitter
- Difference in period between two adjacent clock cycles



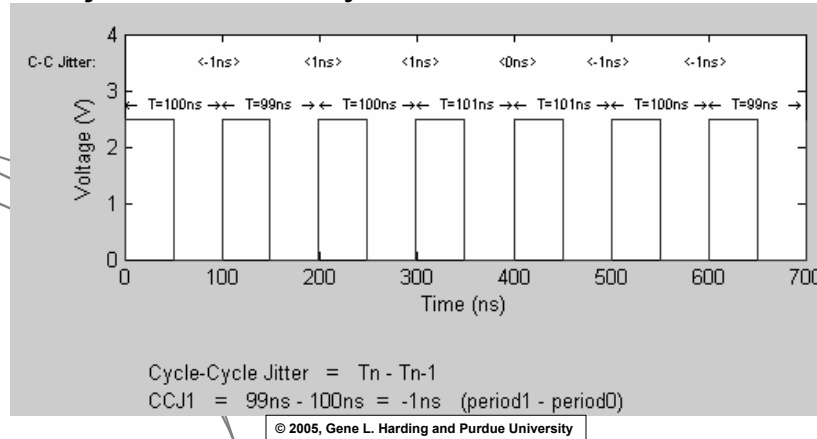
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## Appendix: Lecture Slides

### Jitter Measurements: N-Cycle Jitter

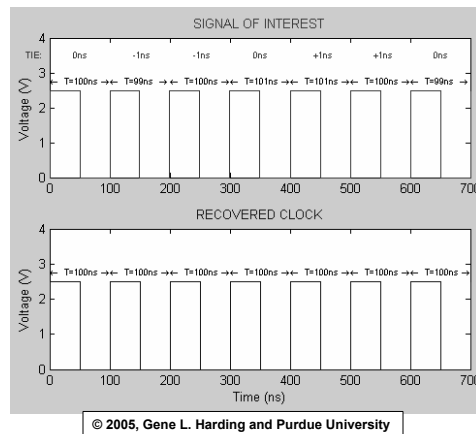
- Similar to cycle-cycle jitter, but non-adjacent clock cycles



7

### Jitter Measurements: Time Interval Error

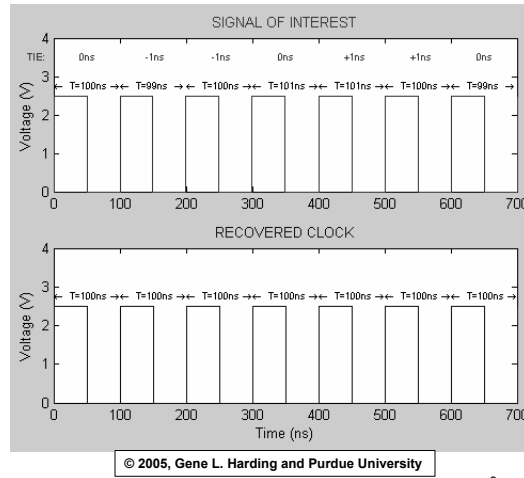
- Requires knowledge of ideal transition times
- Must re-create ideal clock, with HW or SW
- Unit interval (UI)—ideal clock period



8

## Jitter Measurements : Time Interval Error

- Shows cumulative effect of jitter
- When it reaches  $\pm 0.5$  UI, data valid region is closed



9

## Timing Jitter: DSO's Importance

- Jitter characterized using statistics
- Large samples required
- DSOs capture data that can be analyzed

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## Timing Jitter—Review

- What are the two fundamental types of jitter?
  - Random and deterministic
- What is the difference between cycle-cycle and n-cycle jitter?
  - Cycle-cycle jitter compares adjacent clock cycles; n-cycle compares non-adjacent cycles
- To measure TIE, the ideal clock must be re-created. What is the period of this clock called?
  - Unit interval (UI)